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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,229	08/05/2003	Jai P. Bansal	BA-00587	6523

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,229	BANSAL, JAI P.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/06/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/05/2003 and 11/24/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to applicant's Amendment and Remarks filed on 12/06/2004 regarding application 10/634,229 filed on 08/05/2003. Claims 2, 6 and 9 – 12 have been cancelled without prejudice. Claims 1, 3 – 5, 7 and 8 remain pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,710,621 B2 to *Devlin et al.* in view of U.S. Patent No. 6,091,090 to *Gheewala*.

4. As to Claim 1, *Devlin et al.* teach the following subject matter:

- *Field programmable gate array* (FPGA) integrated circuit having *application dependent power supply requirements* – [col. 1, line 15 – 17]; *Programmable power supply* for FPGA chips and ASICs – [col. 7, line 17 – 23]; *FPGA can be an ASIC* – [col. 7, line 36 – 39]; Notice that (1) *gate array* is a *logic cell array*, (2) FPGA is built of *logic cells*, and it can be designed as an *application specific integrated circuit* (ASIC) device; Therefore, *FPGA* can be a *cell-based ASIC device*;

- A *FPGA* (*ASIC*) built from a *Core Logic* and many *I/O Pin Banks* requiring (*different processing/switching speeds*) and *different voltage levels* (i.e., *different power supply voltages*) – [Fig. 2; col. 2, line 56 – 59]; Notice that the (1) *Core Logic* and *I/O Pin Banks* are *logic blocks* which performs *different logic functions* (e.g., data processing, data transmit and/or receive), (2) *logic gates* (i.e., NAND, NOR, INV) *like power supply voltages* are grouped into respective *logic blocks*, (3) *logic gates* of like processing/switching speed have *like power supply voltages*, (4) *logic gates* (NAND, NOR, INV) are *circuit macros*;
- *Industry electrical signal standards* include: *transistor-transistor logic (TTL)*, *complementary metal oxide semiconductor (CMOS)*, *low voltage differential signaling (LVDS)*, *low voltage positive emitter coupled logic (LVPECL)*, and *gunning transceiver logic (GTL)* – [col. 2, line 33 – 42]; Notice that *logic gates* in each *standard* (i.e., sub-library) have like *processing/switching speed* and *like power supply voltages*; Notice that the *Core Logic* and *I/O Pin Banks* (logic blocks) are synthesized using the *logic circuit macros* in the *industry electrical signal standards* (i.e., *sub-libraries*) corresponding to respective *power supply voltages* (e.g., V_{core}, V_{io}) for the *Core Logic* and *I/O Pin Banks*, respectively.

Devlin et al. teach all the subject matter given above; they do not teach a method of reserving *metal layer M1* for power supply bus when developing a bus structure of ASIC device image. But *Gheewala* discloses that *power supply trace* (i.e., *power supply bus*) is implemented *metal one (M1) layer* for coupling *power supply source VDD* – [col. 1, line 65 – col. 2, line 3].

Gheewala also discloses the following subject matter:

- *Power routing technique* for *gate array (integrated circuit) design* – [title; abstract]; Notice that an *ASIC device* is a *gate array (integrated circuit) design;*
- *Macro cells* are constructed using *(logic) elements* such as NAND gates, NOR gates – [col. 1, line 24 – 25];
- A designer selected desired elements from a *library of macro cells* and placed them in a design. The *macro cells* may be *interconnected* (i.e., *synthesized*)

in a variety ways (into logic blocks) to performed desired functions – [col. 1, line 25 – 29];

- *M1 layer* has been used in *route power supply traces* and other *global interconnections* – [col. 2, line 14 – 16]; Notice that the M1 layer is reserved for *power supply bus* when developing a bus structure of ASIC device image.

In addition, *Gheewala* discloses that an advantage of reserving the M1 metal layer for power supply trace is that a direct connection can be made between power supply trace and diffusion regions without additional metal routing – [col. 2, line 8 – 13].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Gheewala* in reserving *metal layer M1* as *power supply trace* (*power supply bus*) when developing a bus structure of ASIC device image in order to achieve a *direct connection between power supply trace and diffusion regions* of *logic circuit macros* (*macro cells*) utilizing different power supply voltages without additional metal routing.

Notice that *power supply trace* (*power supply bus*) are added to *metal layer M1* in the *Core Logic* and *I/O Pin Banks* (logic blocks) in order to providing them requiring power supply voltages.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

5. As to Claim 5, reasons are included in **[Response A]** given above. Notice that the explanations included in **[Response A]** could be applied in generating a computer program product comprising a set of *program code means* as recited in Claim 5.

6. As to Claims 4 and 8, *Devlin et al.* teach the following subject matter:

- *Power control circuit 80* is coupled to individual power supplies for setting (levels of) their *output voltages*– [Fig. 3; col. 8, line 10 – 12];
- *Programmable Power Supply* using *DC-to-DC converter* – [col. 11, line 12 – 26; Table 1]

Notice that both *power control circuit* and *programmable power supply* utilize a *level converter* having *multiple power supply voltages*.

7. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,710,621 B2 to *Devlin et al.* in view of U.S. Patent No. 6,091,090 to *Gheewala* over U.S. Patent Application Publication No. 2003/0101307 A1 to *Gemelli et al.*

8. As to Claim 3 and 7, *Devlin et al.* and *Gheewala* teach all subject matter recited in Claim 1, they do not teach a method of including a customer *intellectual property (IP) macro* in a *ASIC device*. But *Gemelli et al.* disclose this method in Paragraph 0002 and Paragraph 0003. *Gemelli et al.* disclose the following subject matter:

- *Macro-cell based design* implement on a *ASIC* (i.e., *cell-based ASIC device*) – [Paragraph 0018];
- *Macro-cells* can be either *developed by user* or bought on the market as *Intelligent Properties* (*IP*) – [Paragraph 0003]; Notice that an *IP macro* developed by a user for a specific application is a *custom IP macro*;
- *Microprocessor interfaces and local bus interfaces are realized with different macro- cells* – [Paragraph 0036];

Notice that the *custom IP macro* is contained in the *logic blocks* of an *ASIC device* in order to realize *microprocessor interface* and/or *local bus interface* of the *ASIC device* based on specifications uniquely defined by the end user.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Gemelli et al.* in including a *custom IP macro* in the *logic blocks* of an *ASIC device* in order to realize *microprocessor interface* and/or *local bus interface* of the *ASIC device* based on specifications uniquely defined by the end user.

Response to Amendment and Remarks

9. Applicant's amendment and remarks filed on 12/06/2004 have been reviewed. Applicant's arguments have been fully considered but they are not persuasive. Key arguments and their response related to the claims are listed as below:

[Argument 1]: Prior art (U.S. Patent No. 6,710,621 B2 to *Devlin et al.*) does not teach or suggest "*grouping circuit macro of like power supply voltages into respective logic blocks*":

[Response 1]: *Devlin et al.* do disclose *Industry electrical signal standards* which include *transistor-transistor logic* (TTL), *complementary metal oxide semiconductor* (CMOS), *low voltage differential signaling* (LVDS), *low voltage positive emitter coupled logic* (LVPECL), and *gunning transceiver logic* (GTL) – [col. 2, line 33 – 42]; Notice that (1) voltage (bias) requirement for one standard is nominally different from that of another standard (2) logic blocks in one standard have *like processing/switching speed* and *like power supply voltages* in order to achieve good compatibility (3) the Core Logic and I/O Pin Banks (logic blocks) are synthesized using *many* logic blocks (logic circuit macros) of the same standard (e.g., TTL). Therefore, *Devlin et al.* implicitly disclose grouping circuit macros of like power supply voltages into respective logic blocks.

[Argument 2]: *Gheewala* (U.S. Patent No. 6,091,090) teaches gate level macro cells which is at a lower level than *Devlin's* "core logic"

[Response 2]: *Gheewala* teaches gate array *integrated circuit* – [abstract]. Notice gate array integrated circuit is an integrated circuit built of gate array; it can be any logic circuit/block (e.g., core logic).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272-1899. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 305-3413 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Patent Examiner
Art Unit 2825
February 11, 2005

A. M. Thompson
Primary Examiner
Technology Center Z800